GAUNTLET

Schematic Package Supplement to the
Gauntlet™ Operators Manual

© 1985 Atari Games Corporation. All rights reserved.

NOTE

In the schematics printed on Sheets 1-16
a slash (/) in front of a signal name indicates
an active low signal. In the signal name
glossary (printed at the end of this sche-
matic package) these signals are over-
scored, e.g., COMPSYNC.
Table of Contents

Gauntlet™ PCB Schematic Diagram .................................................. Sheets 1-16
Audio PCB Assembly Schematic Diagram (U.S.) ............................... Sheet 17
Regulator/Audio III PCB Schematic Diagram (Ireland) ....................... Sheet 18
Switching/Linear (SL) Power Supply Wiring Diagram (U.S.) ............... Sheet 19
Linear Power Supply Wiring Diagram (Ireland) .................................. Sheet 20
Gauntlet Game Wiring Diagram ..................................................... Sheet 21
Coin Door Wiring Diagram ............................................................. Sheet 22
Gauntlet 68010 and 6502 Microprocessor Memory Maps ..................... Sheet 23
Gauntlet Signal Name Glossary ...................................................... Sheets 24-25
Gauntlet™ Game PCB
Schematic Diagram
NOTICE TO ALL PERSONS RECEIVING THIS DRAWING:
CONFIDENTIAL: Reproduction forbidden without the specific written permission of Atari Games Corporation, Sunnyvale, CA. This drawing is only conditionally issued, and neither receipt nor possession thereof confers or transfers any rights in, or license to use, the subject matter of the drawing or any design or technical information shown thereon, nor any right to reproduce this drawing or any part thereof. Except for manufacture by vendors of Atari Games Corporation, and for manufacture under the corporation's written license, no right is granted to reproduce this drawing or the subject matter thereof, unless by written agreement with or written permission from the corporation.

Gauntlet™ Game PCB Schematic Diagram

© 1985 Atari Games Corporation

SP-284 Sheet 12
1st printing
Gauntlet™ Game PCB
Schematic Diagram

NOTICE TO ALL PERSONS RECEIVING THIS DRAWING
CONFIDENTIAL: Reproduction forbidden without the specific written permission of Atari Games Corporation, Sunnyvale, CA. This drawing is only conditionally issued, and neither receipt nor possession thereof confers or transfers any right to, or license to use, the subject matter of the drawing or any design or technical information shown therein, nor any right to reproduce this drawing or any part thereof. Except for manufacture by vendors of Atari Games Corporation, and for manufacture under the corporation's written license, no right is granted to reproduce this drawing or the subject matter thereof, unless by written agreement with or written permission from the corporation.
NOTICE TO ALL PERSONS RECEIVING THIS DRAWING
CONFIDENTIAL: Reproduction forbidden without the specific written permission of Atari Games Corporation, Sunnyvale, CA. This drawing is only conditionally issued, and neither receipt nor possession thereof conveys or transfers any right to, or license to use, the subject matter of the drawing or any design or technical information shown therein, nor any right to reproduce this drawing or any part thereof. Except for manufacture by vendors of Atari Games Corporation, and for manufacture under the corporation's written license, no right is granted to reproduce this drawing or the subject matter thereof, unless by written agreement with or written permission from the corporation.

Gauntlet™ Game PCB
Schematic Diagram

SP-284 Sheet 15
1st printing

© 1985 Atari Games Corporation
NOTICE TO ALL PERSONS RECEIVING THIS DRAWING
CONFIDENTIAL. Reproduction forbidden without the specific written permission of Atari Games Corporation, Sunnyvale, CA. This drawing is only conditionally issued, and neither receipt nor possession thereof confers or transfers any right to, or license to, use, the subject matter of the drawing or any design or technical information shown therein, nor any right to reproduce this drawing or any part thereof. Except for manufacture by vendors of Atari Games Corporation, and for manufacture under the corporation's written license, no right is granted to reproduce this drawing or the subject matter thereof, unless by written agreement with or written permission from the corporation.

Gauntlet™ Game Wiring Diagram

SP-284 Sheet 21
1st printing

© 1985 Atari Games Corporation
COIN DOOR WIRING DIAGRAM

NOTICE TO ALL PERSONS RECEIVING THIS DRAWING
CONFIDENTIAL. Reproduction forbidden without the specific written permission of Atari Games Corporation, Sunnyvale, CA. This drawing is only conditionally issued, and neither receipt nor possession thereof conveys or transfers any right in, or license to use, the subject matter of the drawing or any design or technical information shown thereon, nor any right to reproduce this drawing or any part thereof. Except for manufacture by vendees of Atari Games Corporation, and for manufacture under the corporation's written license, no right is granted to reproduce this drawing of the subject matter thereof, unless by written agreement with or written permission from the corporation.
# Gauntlet™ 6502 Memory Map

<table>
<thead>
<tr>
<th>FUNCTION</th>
<th>ADDRESS</th>
<th>R/W</th>
<th>DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Program RAM</td>
<td>0000-0FFF</td>
<td>R/W</td>
<td>D0-D7</td>
</tr>
<tr>
<td>Write 68010 Port (Output Buffer)</td>
<td>1000</td>
<td>W</td>
<td>D0-D7</td>
</tr>
<tr>
<td>Read 68010 Port (Input Buffer)</td>
<td>1010</td>
<td>R</td>
<td>D0-D7</td>
</tr>
<tr>
<td><strong>Audio Mix:</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Speech Mix</td>
<td>1020</td>
<td>W</td>
<td>D5-D7</td>
</tr>
<tr>
<td>Effects Mix</td>
<td>1020</td>
<td>W</td>
<td>D3, D4</td>
</tr>
<tr>
<td>Music Mix</td>
<td>1020</td>
<td>W</td>
<td>D0-D2</td>
</tr>
<tr>
<td>Coin 1 (Left)</td>
<td>1020</td>
<td>R</td>
<td>D3</td>
</tr>
<tr>
<td>Coin 2</td>
<td>1020</td>
<td>R</td>
<td>D2</td>
</tr>
<tr>
<td>Coin 3</td>
<td>1020</td>
<td>R</td>
<td>D1</td>
</tr>
<tr>
<td>Coin 4 (Right)</td>
<td>1020</td>
<td>R</td>
<td>D0</td>
</tr>
<tr>
<td>Data Available (@ 1010) (Active High)</td>
<td>1030</td>
<td>R</td>
<td>D7</td>
</tr>
<tr>
<td>Output Buffer Full (@ 1000) (Active High)</td>
<td>1030</td>
<td>R</td>
<td>D6</td>
</tr>
<tr>
<td>Speech Ready (Active Low)</td>
<td>1030</td>
<td>R</td>
<td>D5</td>
</tr>
<tr>
<td>Self-Test (Active Low)</td>
<td>1030</td>
<td>R</td>
<td>D4</td>
</tr>
<tr>
<td>Music Reset (Low Reset)</td>
<td>1030</td>
<td>W</td>
<td>D7</td>
</tr>
<tr>
<td>Speech Write (Active Low)</td>
<td>1031</td>
<td>W</td>
<td>D7</td>
</tr>
<tr>
<td>Speech Reset (Active Low)</td>
<td>1032</td>
<td>W</td>
<td>D7</td>
</tr>
<tr>
<td>Speech Squeak (Low = 650KHz Clock)</td>
<td>1033</td>
<td>W</td>
<td>D7</td>
</tr>
<tr>
<td>Coin Counter Right (Active High)</td>
<td>1034</td>
<td>W</td>
<td>D7</td>
</tr>
<tr>
<td>Coin Counter Left (Active High)</td>
<td>1035</td>
<td>W</td>
<td>D7</td>
</tr>
<tr>
<td>Effects</td>
<td>1800-180F</td>
<td>R/W</td>
<td>D0-D7</td>
</tr>
<tr>
<td>Music</td>
<td>1810-1811</td>
<td>R/W</td>
<td>D0-D7</td>
</tr>
<tr>
<td>Speech</td>
<td>1820</td>
<td>W</td>
<td>D0-D7</td>
</tr>
<tr>
<td>Interrupt Acknowledge</td>
<td>1830</td>
<td>R/W</td>
<td>xx</td>
</tr>
<tr>
<td>Program ROM (48k bytes)</td>
<td>4000-FFFF</td>
<td>R</td>
<td>D0-D7</td>
</tr>
</tbody>
</table>

**NOTICE TO ALL PERSONS RECEIVING THIS DRAWING**

CONFIDENTIAL. Reproduction forbidden without the specific written permission of Atari Games Corporation, Sunnyvale, CA. This drawing is solely conditionally issued, and neither receipt nor possession thereof conveys or transfers any right in, or license to use, the subject matter of the drawing or any design or technical information shown therein, nor any right to reproduce this drawing or any part thereof. Except for manufacture by vendors of Atari Games Corporation, and for manufacture under the corporation's written license, no right is granted to reproduce this drawing or the subject matter thereof, unless by written agreement with or written permission from the corporation.
**Gauntlet™ 68010 Memory Map**

<table>
<thead>
<tr>
<th>FUNCTION</th>
<th>ADDRESS</th>
<th>R/W</th>
<th>DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Program ROM/Operating System</td>
<td>000000–00FFFF</td>
<td>R</td>
<td>D0–D15</td>
</tr>
<tr>
<td>Program ROM/SLAPSTIC</td>
<td>038000–03FFFF</td>
<td>R</td>
<td>D0–D15</td>
</tr>
<tr>
<td>Program ROM/Main</td>
<td>040000–07FFFF</td>
<td>R</td>
<td>D0–D15</td>
</tr>
<tr>
<td>Spare RAM</td>
<td>800000–801FFF</td>
<td>R/W</td>
<td>D0–D15</td>
</tr>
<tr>
<td>EEPROM</td>
<td>802001–802FFF</td>
<td>R/W</td>
<td>D7–D0</td>
</tr>
<tr>
<td>Player 1 Input (see detail below)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Player 2 Input</td>
<td>803001</td>
<td>R</td>
<td>D0–D71</td>
</tr>
<tr>
<td>Player 3 Input</td>
<td>803003</td>
<td>R</td>
<td>D0–D7</td>
</tr>
<tr>
<td>Player 4 Input</td>
<td>803005</td>
<td>R</td>
<td>D0–D7</td>
</tr>
<tr>
<td>Player Inputs:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Joystick Up</td>
<td></td>
<td></td>
<td>D7</td>
</tr>
<tr>
<td>Joystick Down</td>
<td></td>
<td></td>
<td>D6</td>
</tr>
<tr>
<td>Joystick Left</td>
<td></td>
<td></td>
<td>D5</td>
</tr>
<tr>
<td>Joystick Right</td>
<td></td>
<td></td>
<td>D4</td>
</tr>
<tr>
<td>Spare</td>
<td></td>
<td></td>
<td>D3</td>
</tr>
<tr>
<td>Spare</td>
<td></td>
<td></td>
<td>D2</td>
</tr>
<tr>
<td>Fire</td>
<td></td>
<td></td>
<td>D1</td>
</tr>
<tr>
<td>Magic/Start</td>
<td></td>
<td></td>
<td>D0</td>
</tr>
<tr>
<td>VBLANK (Active Low)</td>
<td>803009</td>
<td>R</td>
<td>D6</td>
</tr>
<tr>
<td>Output/Buffer Full (@ 803170) (Active High)</td>
<td>803009</td>
<td>R</td>
<td>D5</td>
</tr>
<tr>
<td>Input/Buffer Full (@ 80300F) (Active High)</td>
<td>803009</td>
<td>R</td>
<td>D4</td>
</tr>
<tr>
<td>Self-Test (Active Low)</td>
<td>803009</td>
<td>R</td>
<td>D3</td>
</tr>
<tr>
<td>Read Sound Processor (6502)</td>
<td>80300F</td>
<td>R</td>
<td>D0–D7</td>
</tr>
<tr>
<td>Watchdog (128 msec. timeout)</td>
<td>803100</td>
<td>W</td>
<td>xx</td>
</tr>
<tr>
<td>LED-1 (Low On)</td>
<td>803121</td>
<td>W</td>
<td>D0</td>
</tr>
<tr>
<td>LED-2 (Low On)</td>
<td>803123</td>
<td>W</td>
<td>D0</td>
</tr>
<tr>
<td>LED-3 (Low On)</td>
<td>803125</td>
<td>W</td>
<td>D0</td>
</tr>
<tr>
<td>LED-4 (Low On)</td>
<td>803127</td>
<td>W</td>
<td>D0</td>
</tr>
<tr>
<td>Sound Processor Reset (Low Reset)</td>
<td>80312F</td>
<td>W</td>
<td>D0</td>
</tr>
<tr>
<td>VBlank Acknowledge</td>
<td>803140</td>
<td>W</td>
<td>xx</td>
</tr>
<tr>
<td>Unlock EEPROM</td>
<td>803150</td>
<td>W</td>
<td>xx</td>
</tr>
<tr>
<td>Write Sound Processor (6502)</td>
<td>803171</td>
<td>W</td>
<td>D0–D7</td>
</tr>
<tr>
<td>Playfield RAM</td>
<td>900000–901FFF</td>
<td>R/W</td>
<td>D0–D15</td>
</tr>
<tr>
<td>Motion Object Picture</td>
<td>902000–9027FF</td>
<td>R/W</td>
<td>D0–D15</td>
</tr>
<tr>
<td>Motion Object Horizontal Position</td>
<td>902800–902FFF</td>
<td>R/W</td>
<td>D0–D15</td>
</tr>
<tr>
<td>Motion Object Vertical Position</td>
<td>903000–9037FF</td>
<td>R/W</td>
<td>D0–D15</td>
</tr>
<tr>
<td>Motion Object Link</td>
<td>903800–903FFF</td>
<td>R/W</td>
<td>D0–D15</td>
</tr>
<tr>
<td>Spare RAM</td>
<td>904000–904FFF</td>
<td>R/W</td>
<td>D0–D15</td>
</tr>
<tr>
<td>Alphanumericics RAM</td>
<td>905000–905FFF</td>
<td>R/W</td>
<td>D0–D15</td>
</tr>
<tr>
<td>Playfield Vertical Scroll</td>
<td>905F6E, 905F6F</td>
<td>R/W</td>
<td>D7–D15</td>
</tr>
<tr>
<td>Playfield ROM Bank Select</td>
<td>905F6F</td>
<td>R/W</td>
<td>D0, D1</td>
</tr>
<tr>
<td>Color RAM Alpha</td>
<td>910000–9101FF</td>
<td>R/W</td>
<td>D0–D15</td>
</tr>
<tr>
<td>Color RAM Motion Object</td>
<td>910200–9103FF</td>
<td>R/W</td>
<td>D0–D15</td>
</tr>
<tr>
<td>Color RAM Playfield Shadow</td>
<td>910400–9104FF</td>
<td>R/W</td>
<td>D0–D15</td>
</tr>
<tr>
<td>Color RAM Playfield</td>
<td>910500–9105FF</td>
<td>R/W</td>
<td>D0–D15</td>
</tr>
<tr>
<td>Color RAM (Spare)</td>
<td>910600–9107FF</td>
<td>R/W</td>
<td>D0–D15</td>
</tr>
<tr>
<td>Playfield Horizontal Scroll</td>
<td>930000, 930001</td>
<td>W</td>
<td>D0–D8</td>
</tr>
</tbody>
</table>

**NOTE**

All addresses can be accessed in byte or word mode.
Gauntlet Signal Name Glossary, continued

HSIZO–HSIZ2
HSYNC, HSYNC
INPUT
INT0–INT3
IOUT0–IOUT3
LATCH
LAUD
LBA0–LBA8
LBB0–LBB8
LBCKF
LBCKR
LDBA0–LDBA7
LDBB0–LDBB7
LDA
LDAB
LD
LD5
LED1–LED4
LEFT1–LEFT4
LINK
LMPS
LNK0–LNK9
MA1–MA14
MATCH
MATCHDL
MBUS
MC0, MC1
MCEN
MCKF
MCKR
MD0–MD15
MFLP
Motion object horizontal size
Horizontal sync output
68010 miscellaneous inputs buffer select
Color intensity RAM data
Intensity latched digital video output
68010 miscellaneous latched outputs chip select
Summed left channel audio
Line buffer "A" address bus
Line buffer "B" address bus
Line buffer clock inverted phase
Line buffer clock
Line buffer "A" data bus
Line buffer "B" data bus
Load line buffer "A" address counters
Load line buffer "A" or "B" address counters
Load line buffer "B" address counters
68010 lower data strobe
LED outputs, players 1–4
Joystick left switch inputs, players 1–4
Latch motion object link data
Stop motion object processing for line buffer changeover
Motion object link data
68010 address bus buffered
Motion object H and V data matches current playfield position
Previous MATCH state
68010 "M" data bus buffers enable
Motion object parameter control select
Motion object parameter control enable
Master clock, inverted phase
Master clock
68010 "M" data bus
Motion object horizontal flip parameter
MIX
MO/PF
MOHI, MOLO
MOSR0–MOSR3
MOSR4–MOSR7
MPICO–MPIC7
MPX0–MPX7
MREFI
MUSIC
NEWMO
NXL, NXL
(NXL*)
NXLDL
PF1LD–PF256LD
PF1V–PF256V
PF8H–PF256H
PF80K0, PF80K1
PFH1, PFLO
PFHIST
PF_S0–PF8R3
PF8R4–PF8R6
PF0X–PF0X6
PICST0–PICST7
PICT
PICTDL
PKAUL
PL1–PL4
PM0–PM2
POKEY
PR1–PR6
R/W
Latch audio mix data
Motion object or playfield picture select
Motion object RAM chip selects
Motion object pixel data, before the line buffers
Motion object pixel palette data, before the line buffers
The lower 8 bits of the motion object picture address
Motion object pixel data, after the line buffers
Motion object stamp horizontal flip state
Music chip select
Start a new motion object
Next line
NXL one clock cycle early
NXL delayed one clock cycle
Latched playfield horizontal scroll data
Playfield vertical address counter chain
Playfield horizontal address counter chain
Playfield picture bank select
Playfield RAM chip selects
Playfield scroll control
Playfield pixel data, before PF5H
Playfield pixel palette data, before PF5H
Playfield pixel data after PF5H
Motion object picture start address
Latch motion object picture data
PICT delayed one clock cycle
Effects chip audio
Player input chip selects, players 1–4
Effects audio mix control bits
Effects chip select
Pull-up resistors
68010 read/write control, unbuffered

NOTICE TO ALL PERSONS RECEIVING THIS DRAWING
CONFERENTIAL Reproduction forbidden
without the specific written permission of Atari
Games Corporation, Sunnyvale, CA. This draw-
ing is only conditionally issued, and neither re-
cipient nor possession thereof conveys or transfers any right to, or license to use, the sub-
ject matter of the drawing or any design or tech-
nical information shown therein, nor any right
or other person to reproduce this drawing or any part thereof. Except for manufacturing by vendors of Atari
Games Corporation, and for manufacture under
the corporation's written license, no right is granted to reproduce this drawing or the sub-
ject matter thereof, unless by written agree-
ment with or written permission from the
corporation.
Gauntlet Signal Name Glossary

2.5V
+5AUD
10.5V
+12V
+15V
−15V
−5V
1H−256H
1V−128V
4H
4HD3, 4HD3
4HDD
4HDL
68KBUF
A1−A23
ACS
ALC3, ALC4
ALHI, ALLO
APIX0, APIX1
A$5
AUDIO−L, AUDIO−R
B02
BAS
BCS
BLU0−BLU3
BLUE
BOUT0−BOUT3
BR/W
BUFCLR
BW/R
CA5, CA7
CCTR1, CCTR2
CLR A
CLR B

2.5 volts audio amplifier reference
5 volts audio amplifier reference
Power-on-reset control voltage
+ 12 volts regulated
+ 15 volts unregulated
− 15 volts unregulated
− 5 volts regulated
Screen horizontal address counter chain
Screen vertical address counter chain
Inverted 4H signal
4H signal delayed three clock cycles
4H signal delayed two clock cycles
4H signal delayed one clock cycle
68010 output buffer full to (6502)
68010 address bus unbuffered
‘A’ line buffer RAMs chip select
Alphanumeric palette data bits 3 and 4
Alphanumeric RAM chip selects
Alphanumeric pixel data
68010 address strobe
Left and right audio outputs (5V peak-to-peak)
6502 buffered phase 2 (Φ2)
Buffered address strobe (see A5)
“B” line buffer RAMs chip select
Blue color RAM data
Blue analog video output
Blue latched digital video output
68010 read/write control, buffered
Swap “A” and “B” line buffers, clear line buffer counter chain
68010 read/write inverted, buffered
Color RAM address bits 5 and 7
Coin counter outputs 1 and 2,
Clear line buffer “A” address counters
Clear line buffer “B” address counters

COIN
COIN1−L, COIN2,
COIN3, COIN4−R
COMP SYNC
CRA0−CRA9
CRAM, CRAM
CRAMWR
D0−D15
DOWN−1−
DOWN−4
EE PROM
END
FCLOCK
FIRE−1−FIRE−4
FLBA
FLBB
GCS0−GCS5
GLD
GND
GOUT0−GOUT3
GP0−GP14
GP1V, GP2V,
GP4V
GPEN
GREEN
GRH/L
GRN0−GRN3
H03
HFLP
HOR Z
HORIZDL
HORIZDL
HPOS0−HPOS8
HSCRDL

Coin input buffer chip select
Four coin switch inputs
Negative composite sync output
Color RAM address
68010 address decode for color RAM
Color RAM write enable
68010 data bus, unbuffered
Joystick down switch inputs, players 1−4
Electrically erasable PROM chip select
Current motion object finished
System clock inverted phase
Fire switch inputs, players 1−4
Line buffer “A” fill control
Line buffer “B” fill control
Graphics ROMs chip select
Graphics load (to SLAGS chips)
System ground
Green latched digital video output
Graphics picture address
Graphics picture stamp sub-address
Graphics picture enable
Green analog video output
Graphics ROM high/low select (A14 on a 27256)
Green color RAM data
Alphanumeric load (to shift registers)
Graphics stamp horizontal flip
Latch motion object horizontal data and palette data
HORIZ delayed one clock cycle
Motion object horizontal position data
Latch playfield horizontal scroll data

NOTE
In this signal name glossary all active-low signals are overscored, e.g., COMPSYNC. In the schematics printed on Sheets 1−16 a slash (/) in front of a signal name indicates an active-low signal.
Gauntlet Signal Name Glossary, continued

V BUS 68010 "V" bus enable (for video RAM)
V CC System Vcc (5 volts regulated)
V CPU 68010-to-video-RAM synchronization control
VERT Latch motion object vertical data and size data
VERTDL VERT delayed one clock cycle
VERTDL VIDBLANK Video blank (horizontal and vertical blank mixed)
VMATCH Motion object vertical parameter matches current playfield vertical position
VOICE Speech chip select
V P0S0–V P0S8 Motion object vertical position data
V RA0–V RA11 Video RAM address bus
V RAM 68010 address decode for video RAM
V RAM RD 68010 read from video RAM
V RAM WE 68010 write to video RAM
V RD0–VRD15 Video RAM data bus, unbuffered
V RDTACK Video RAM to 68010 data acknowledge
V SIZ0–VSIZ2 Motion object vertical size parameter
V SYNC, V SYNC Vertical sync
W DOG Watchdog control
W H 68010 write high byte
W L 68010 write low byte
W RG8K 6502 write to output buffer (to 68010)
Y AMRES Music chip reset
Y MO–YM2 Music audio mix control bits
Z REF Intensity reference for video output
Gauntlet Signal Name Glossary, continued

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAM0, RAM1</td>
<td>68010 working RAM chip selects</td>
</tr>
<tr>
<td>RAUD</td>
<td>Summed right channel audio</td>
</tr>
<tr>
<td>RCLK</td>
<td>System clock</td>
</tr>
<tr>
<td>RD0–RD15</td>
<td>68010 ROM data bus</td>
</tr>
<tr>
<td>RD68K</td>
<td>6502 read 68010 output buffer</td>
</tr>
<tr>
<td>RED</td>
<td>Red analog video output</td>
</tr>
<tr>
<td>RED0–RED3</td>
<td>Red color RAM data</td>
</tr>
<tr>
<td>RIGHT-1–4</td>
<td>Joystick right switch inputs, players 1–4</td>
</tr>
<tr>
<td>ROM</td>
<td>68010 ROM data bus enable</td>
</tr>
<tr>
<td>ROM0–ROM4</td>
<td>68010 program ROM chip selects</td>
</tr>
<tr>
<td>ROMH/L</td>
<td>68010 program ROM high/low select (A14 on a 27256)</td>
</tr>
<tr>
<td>ROUT0–ROUTE3</td>
<td>Red latched digital video output</td>
</tr>
<tr>
<td>SA0–SA15</td>
<td>6502 address bus unbuffered</td>
</tr>
<tr>
<td>SBA0–SBA13</td>
<td>6502 buffered address bus</td>
</tr>
<tr>
<td>SBD0–SBD7</td>
<td>6502 buffered data bus</td>
</tr>
<tr>
<td>SBR/WR</td>
<td>6502 buffered read/write control</td>
</tr>
<tr>
<td>SBW/R</td>
<td>6502 buffered read/write control inverted</td>
</tr>
<tr>
<td>SD0–SD7</td>
<td>6502 data bus unbuffered</td>
</tr>
<tr>
<td>SELFTEST</td>
<td>Self-test switch input test pad</td>
</tr>
<tr>
<td>SID</td>
<td>Serial input data</td>
</tr>
<tr>
<td>SIORD</td>
<td>6502 miscellaneous input read control</td>
</tr>
<tr>
<td>SIOWR</td>
<td>6502 output latch control</td>
</tr>
<tr>
<td>SIRQACK</td>
<td>6502 interrupt acknowledge</td>
</tr>
<tr>
<td>SLAPSTK</td>
<td>SLAPSTIC chip select</td>
</tr>
<tr>
<td>SM0–SM2</td>
<td>Speech audio mix control bits</td>
</tr>
<tr>
<td>SNDBUF</td>
<td>6502 output buffer full (to 68010)</td>
</tr>
<tr>
<td>SNDINT</td>
<td>68010 interrupt from 6502</td>
</tr>
<tr>
<td>SNDIRQ</td>
<td>6502 4-millisecond interrupt</td>
</tr>
<tr>
<td>SNDNM1</td>
<td>6502 non-maskable interrupt</td>
</tr>
<tr>
<td>SNDRD</td>
<td>6502 read buffer from 6502</td>
</tr>
<tr>
<td>SNDRES</td>
<td>6502 master reset (controlled by 68010)</td>
</tr>
<tr>
<td>SNDWR</td>
<td>65010 write to output buffer (to 6502)</td>
</tr>
<tr>
<td>SOD</td>
<td>Serial output data</td>
</tr>
<tr>
<td>SPHRDY</td>
<td>Speech chip ready</td>
</tr>
<tr>
<td>SPHRES</td>
<td>Speech chip reset</td>
</tr>
<tr>
<td>SPHWR</td>
<td>Speech chip write</td>
</tr>
<tr>
<td>SQUEAK</td>
<td>Speech chip operating frequency control</td>
</tr>
<tr>
<td>SRD</td>
<td>6502 read phase</td>
</tr>
<tr>
<td>START-1–START-4</td>
<td>Start switch inputs, players 1–4</td>
</tr>
<tr>
<td>STTEST</td>
<td>Self-test switch input</td>
</tr>
<tr>
<td>SWR</td>
<td>6502 write phase</td>
</tr>
<tr>
<td>SYSRES</td>
<td>System reset (power up)</td>
</tr>
<tr>
<td>UDS</td>
<td>68010 upper data strobe</td>
</tr>
<tr>
<td>UNLOCK</td>
<td>EEPROM write enable control</td>
</tr>
<tr>
<td>UP-1–UP-4</td>
<td>Joystick up switch inputs, players 1–4</td>
</tr>
<tr>
<td>VAS0, VAS1</td>
<td>Video RAM address control</td>
</tr>
<tr>
<td>(VAS0*), (VAS1*)</td>
<td>VAS0 and VAS1 before being latched</td>
</tr>
<tr>
<td>VBD0–VBD15</td>
<td>Video RAM buffered data bus</td>
</tr>
<tr>
<td>VBKACK</td>
<td>Vertical blank interrupt acknowledge</td>
</tr>
<tr>
<td>VGBKNT</td>
<td>Vertical blank interrupt</td>
</tr>
<tr>
<td>VBLANK</td>
<td>Vertical blank</td>
</tr>
</tbody>
</table>